Claims

1. An OR gate circuit, comprising:

a first input;

a second input;

a double-gated field effect transistor including,

a source,

a top gate coupled to the first input,

a bottom gate coupled to the second input, and

a drain; and

an output coupled to the drain.

2. The OR gate circuit of claim 1, wherein the field effect transistor is a PMOS transistor.

3. The OR gate circuit of claim 1, further comprising a precharge transistor coupled to the drain to effect a low voltage on the drain.

4. The OR gate circuit of claim 3, wherein the precharge transistor is a NMOS transistor.

5. An OR gate circuit, comprising

a first input;

a second input;

a double-gated field effect transistor including,

a substrate,

a bottom gate disposed on the substrate and coupled to the second input,

a dielectric disposed on the bottom gate and the substrate,

a channel disposed on the dielectric,

a source disposed on the dielectric and having a source extension extending from the main body of the source and coupled to the channel,

a drain disposed on the dielectric and having a drain extension extending from the main body of the drain and coupled to the channel,

a gate insulator disposed on the channel,

a top gate disposed on the gate insulator and coupled to the first input,

a first spacer disposed between the top gate and the source and proximate to the source extension, and

a second spacer disposed between the top gate and the drain and proximate to the drain extension; and

an output coupled to the drain.

6. The OR gate circuit of claim 5, wherein the field effect transistor is a PMOS transistor.

7. The OR gate circuit of claim 5, further comprising a precharge transistor coupled to the drain to effect a low voltage on the drain.

8. The OR gate circuit of claim 7, wherein the precharge transistor is a NMOS transistor.

9. The OR gate circuit of claim 5, wherein the channel has a cross-sectional U-shape.

10. The OR gate circuit of claim 5, wherein the gate insulator has a cross-sectional U-shape.

11. The OR gate circuit of claim 5, wherein the channel is undoped.

12. The OR gate circuit of claim 5, further comprising a plurality of exterior spacers disposed on the substrate and proximate to the dielectric layer, source, and drain.

13. The OR gate circuit of claim 12, further comprising an insulator layer disposed on the substrate and coupled to the exterior spacers.

14. A NOR gate circuit, comprising:

a first input;

a second input;

a double-gated field effect transistor including,

a source,

a top gate coupled to the first input,

a bottom gate coupled to the second input, and

a drain; and

an output coupled to the drain.

15. The NOR gate circuit of claim 14, wherein the field effect transistor is an NMOS transistor.

16. The NOR gate circuit of claim 14, further comprising a precharge transistor coupled to the drain to effect a high voltage on the drain.

17. The NOR gate circuit of claim 16, wherein the precharge transistor is a PMOS transistor.

18. A NOR gate circuit, comprising

a first input;

a second input;

a double-gated field effect transistor including,

a substrate,

a bottom gate disposed on the substrate and coupled to the second input,

a dielectric disposed on the bottom gate and the substrate,

a channel disposed on the dielectric,

a source disposed on the dielectric and having a source extension extending from the main body of the source and coupled to the channel,

a drain disposed on the dielectric and having a drain extension extending from the main body of the drain and coupled to the channel,

a gate insulator disposed on the channel,

a top gate disposed on the gate insulator and coupled to the first input,

a first spacer disposed between the top gate and the source and proximate to the source extension, and

a second spacer disposed between the top gate and the drain and proximate to the drain extension; and

an output coupled to the drain.

19. The NOR gate circuit of claim 18, wherein the field effect transistor is a NMOS transistor.

20. The NOR gate circuit of claim 18, further comprising a precharge transistor coupled to the drain to effect a high voltage on the drain.

21. The NOR gate circuit of claim 20, wherein the precharge transistor is a PMOS transistor.

22. The NOR gate circuit of claim 18, wherein the channel has a cross-sectional U-shape.

23. The NOR gate circuit of claim 18, wherein the gate insulator has a cross-sectional U-shape.

24. The NOR gate circuit of claim 18, wherein the channel is undoped.

25. The NOR gate circuit of claim 18, further comprising a plurality of exterior spacers disposed on the substrate and proximate to the dielectric layer, source, and drain.

26. The NOR gate circuit of claim 18, further comprising an insulator layer disposed on the substrate and coupled to the exterior spacers.